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| PRE-APPEAL BRIEF REQUEST FOR REVIEW | Docket Number (Optional) | |
| *facsimile transmitted to the USPTO on* | 35399.42 | |

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]	Application Number	Filed
	09/990,753	11/16/2001
on ___4/30/07___	First Named Inventor	
Signature ___Sheli Harris___	Heeloo Chung	
	Art Unit	Examiner
Typed or printed name ___Sheli Harris___	2616	Derrick W. Ferris

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
    Note: No more than five (5) pages may be provided.

I am the

[ ] applicant/inventor.

[ ] assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

[X] attorney or agent of record.
Registration number ___40,013___

[ ] attorney or agent acting under 37 CFR 1.34.

Registration number if acting under 37 CFR 1.34 _____

_____
Signature

James E. Harris
Typed or printed name

512-275-6652
Telephone number

4/30/07
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

[X] *Total of ___one___ forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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PATENT APPLICATION
Do. No. 35399.42

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	§	Docket No.: 35399.42
Heeloo Chung, et al.	§	
	§	Confirmation No.: 3370
Application No.: 09/990,753	§	
	§	Art Unit: 2616
Filed: November 16, 2001	§	
	§	Examiner: Derrick W. Ferris
For: High Efficiency Data	§	
Buffering in a Computer	§	
Network Device	§	

MAIL STOP AF
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Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Responsive to the Final Office Action, dated January 30, 2007, please consider the following remarks in connection with the pre-appeal brief request for review. Review of the final rejection is requested for the following reasons.

1. The Inventor's Declarations and Accompanying Exhibits Support An Actual Reduction to Practice Prior to the Effective Date of the Wynne and Tran References

This appeal is noticed as the culmination of a year-and-a-half-long disagreement between the Examiner and the Applicant regarding whether the factual statements in an inventor's 37 C.F.R. § 1.131 Declarations are to be considered evidence of reduction to practice.

In the present application, two Section 1.131 Declarations[1] have been submitted to swear back of two references (Wynne and Tran, as explained in the Office Action responses). As detailed in the Declarations, prior to the filing of a patent application and prior to the effective date of the references, an application-specific integrated circuit that formed the basic embodiment for the patent application was designed, built, and successfully tested. The

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[1] The second declaration was submitted by the inventor to respond to several objections that the Examiner made to the first declaration.

Examiner continues to disregard facts declared under penalty of perjury by the inventor in these two Declarations, and steadfastly refuses to consider the facts in the declaration along with the facts present in the accompanying Exhibits, despite Patent Office guidance to the contrary, as evidenced by the following quote from the January 30, 2007, Office Action:

> As previously stated, there is no factual evidence found in the affidavit to support the claim recitations. In particular, the inventor or author's explanatory statements found in the declaration are not factual evidence. The examiner further notes that [] upon further review, the examiner's supervisor also agrees with the above statement. Thus the rejection is made for lack of factual evidence provided by the affidavit. (p. 2.)

The refusal by the Examiner to consider the facts in the declaration that point to and explain the pertinent portions of the exhibits is squarely at odds with guidance published by the USPTO:

> The essential thing to be shown under 37 C.F.R. 1.131 is priority of invention and this may be done by any satisfactory evidence of the fact. FACTS, not conclusions, must be alleged. Evidence in the form of exhibits may accompany the affidavit or declaration. Each exhibit relied upon should be specifically referred to in the affidavit or declaration, in terms of what it is relied upon to show.
>
> ....
>
> However, when reviewing a 37 CFR 1.131 affidavit or declaration, the examiner must consider all of the evidence presented in its entirety, including the affidavits or declarations and all accompanying exhibits, records and "notes." An accompanying exhibit need not support all claimed limitations, provided that any missing limitation is supported by the declaration itself.
>
> ....
>
> The affidavit or declaration and exhibits must clearly explain which facts or data applicant is relying on to show completion of his or her invention prior to a particular date...Applicant must give a clear explanation of the exhibits pointing out exactly what facts are established and relied on by applicant...
> (M.P.E.P. § 715.07.I.)

Thus "any satisfactory evidence" of a fact is acceptable, all evidence including declarations and exhibits is to be considered in its entirety, and the Applicant not only may but must give a clear explanation of the exhibits. It is erroneous for the Examiner to consider evidence piecemeal, disregard declaration evidence, and disregard the inventor's declaratory explanations as "arguments."

A few specific errors in the Examiner's application of the examining procedures will now be given. First, the Examiner states, on page 3 of the Office Action and with reference to the second Declaration, that "the examiner found no evidence that Exhibit A teaches at least an input for receiving packets of data, *each packet associated with an output queue or*

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equivalent." The Examiner continues in a lengthy argument, not repeated here, that considers portions of the Exhibit piecemeal and wholly ignores the factual trail provided in the Declaration to link the parts together. The Examiner further erroneously characterizes the Declaration as an "argument," although it is clearly factual and detailed in its presentation.

Applicant respectfully requests that the panel read both declarations in conjunction with the Exhibits to which they refer. In full compliance with the requirements of 37 C.F.R. § 1.131, second Declaration paragraphs 4-10 carefully and factually trace the tagging of packets with a header that is used to associate incoming packets with output queues.

The Examiner concludes this line of argument with the statement that "paragraph 6 [of the declaration] further provides no evidence found prior to July 18, 2001 to support the above claim recitation at issue." This is also incorrect. Paragraph 6 specifically refers to Exhibit A for the packet header format for packets input to the Cougar, which as stated in paragraph 4 is part of the Cougar ASIC specification that existed prior to this date. Furthermore, the first declaration, paragraph 8, states that

> "a 'port pipe' as we use the term is a data flow stream between a Cougar and the switch fabric. According to Exhibit C, on the second day of testing we had a network device operating in a loop including an ingress and an egress Cougar, with over 1 billion error-free packets transmitted."

Exhibit C shows that this loop included the <u>Tiger</u> sending packets to the Cougar, prior to July 18, 2001:

> Here we come. Ripley first port pipe is alive:
> IXIA->Tiger-IngressCougar (with Lynx)->BackplaneSerdes->EgressCougar->Tiger->IXIA
>
> We are setting the IXIA in an infinite loop. So far we have **over 1 billion packets** through the pipe with NO ERROR and no dropping. (Decl. 1, Ex. C at 1, emphasis in original.)

The input for receiving packets is clearly shown on page 1 of Exhibit A, as a "Front End C-Port Interface" in the "data path" from "Tiger." This description is entirely consistent with the patent application description of a lookup engine and C-port blocks that include the physical input ports for the buffer manager, including the description:

> By the time the packets have entered the C-port block 110, they have already been assigned to a particular VOQ by the lookup engine 40 (FIG. 1). The VOQ to which the packet is assigned, as well as other data and commands are present in a header of each packet. (Application, p. 4, l. 31 to p. 5, l. 8.)

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When all of this evidence is considered together, it leads to the inescapable conclusion that, prior to July 18, 2001, the Cougar ASIC had an input for receiving packets, and that the input received data packets associated with output queues. The Cougar ASIC high-level purpose for being is as "a buffer/queue manager ASIC in the Cyclone switch system." (Decl. 2, Ex. A at 1.) The Examiner is essentially arguing, with absolutely no foundation in the evidence, that the inventor built a device that did not follow its own specifications or packet interface requirements and was not used for the specific purpose for which it was designed.

The Examiner also argues that he:

> found no evidence that Exhibit A teaches at least an intermediate storage facility manager configured to assign particular blocks of the intermediate storage facility *to output queues, and store one or more packets associated with output queues into blocks assigned to those output queues* or equivalent for the same reason as mentioned above. In particular, there is no further description with respect to the figure shown on page 12 of the exhibit. Thus it is unclear that "p1a" is a part "a" of a "packet 1" as argued by applicant. (Page 4.)

These statements are irreconcilable with the declared facts. Paragraph 11 of the declaration points the reader to pages 11-15 of Exhibit A. Specifically, starting at section 4.4.3.4 on page 11 and continuing through section 4.4.3.6 on page 13, the discussion centers on treatment of the three pointer arrays (head[q], head_elen[q], and tail[q]) shown in the page 12 Figure. By merely reading the Exhibit A text and looking at the figure (for instance the pointers for queue 0), one can discern that "p1a" is a first part of a packet 1:

> For each queue there is:
> - A head pointer (head[q]), which points to the first chunk in the first packet in the queue.
> - A tail pointer (tail[q]), which points to the last chunk in the last packet in the queue. (Decl. 2, p. 11.)

The inventor has also stated the same fact in his second declaration, at paragraph 11.[2]

Applicant respectfully requests that the panel find the Examiner's reasons for maintaining the present rejections insufficient, and return the application to him for further action on the merits.

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[2] It is noted that a typographical error appears in paragraph 11, where it states that packet p1 includes three chunks p1a, p2a, and p3a. The inventor should have identified chunks p1a, p1b, and p1c with packet p1, consistent with Exhibit A and with his description of packets p2, p3, p4, and p5.